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<u>L33</u>	L32 and decod\$5	185	<u>L33</u>
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<u>L31</u>	l26 and retir\$7	284	<u>L31</u>
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<u>L25</u>	(concurrent\$3 or simultaneous\$3 or parallel\$6 or pipelin\$5)	5181998	<u>L25</u>
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» Key

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Modeling architectural improvements in superscalar processors**
Zhu, Y.; Wong, W.F.;
[High Performance Computing in the Asia-Pacific Region, 2000. Proceedings. The Fourth International Conference/Exhibition on](#)
Volume 1, 14-17 May 2000 Page(s):28 - 30 vol.1
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Modeling architectural improvements in superscalar processors

[Zhu, Y.](#) [Wong, W.F.](#)

Sch. of Comput., Nat. Univ. of Singapore, Singapore;

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Abstract

A model of **superscalar** processors using a network of Multiple-Class-Multiple-Resource queues is described and studied. The model is able to model and study instruction classes, instruction dependencies, the cache, the **branch** unit, the **decoder** unit, the **instruction buffer**, the functional units, the retirement buffer, the retirement unit and instruction issue policy in an integer model. The model has been verified against measured performance and has shown an average error of 5%.

Index Terms

Inspec

Controlled Indexing

[buffer storage](#) [computer architecture](#) [instruction sets](#) [performance evaluation](#) [queueing theory](#)

Non-controlled Indexing

[Multiple-Class-Multiple-Resource queues](#) [architectural improvement modeling](#) [average error](#) [branch unit](#) [central instruction buffer](#) [decoder unit](#) [functional units](#) [instruction classes](#) [instruction dependencies](#) [instruction issue policy](#) [measured performance](#) [retirement buffer](#) [retirement unit](#) [superscalar processors](#)

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